Design of Low Power and Area Efficient 256 Bits Shift Register Using Pulsed Latches

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Abstract – In low-power digital design, especially in shift registers, flip-flops (FF) plays a significant role. In move enrolls, the power utilization of framework clock is assessed to be half of the general framework control. This paper proposes a low-power and territory proficient move enlist utilizing computerized beat locks. The region and power utilization are lessened by supplanting flip-flops with beat hooks. This technique takes care of the planning issue between beat locks using various non-cover deferred beat clock motions rather than the ordinary single beat clock flag. A 256-piece move enroll utilizing beat hooks was created utilizing a 0.18µm CMOS process with VDD = 1.8V. The proposed move enroll spares 37% region and 44% power contrasted with the traditional move enlist with flip-flops. In advanced circuits, a move enroll is a course of flip lemon, having a similar clock, in which the yield of each flip-tumble is associated with the "information" contribution of the following flip-slump in the chain, bringing about a circuit that movements by one position the "bit exhibit" put away in it, moving in the information show at its information and moving out the last piece in the cluster, at each progress of the clock input. All the more by and large, a move enroll might be multidimensional, to such an extent that its "information in" and organize yields are themselves bit exhibits: this is executed basically by running a few move registers of a similar piece length in parallel.

Index Terms – Area-efficient, flip-flop, pulsed clock, pulsed latch, shift register .

1. INTRODUCTION

Flip flops are the fundamental stockpiling components utilized broadly in a wide range of advanced plans. As the element size of CMOS innovation process downsized by Moore's Law, planners can coordinate many quantities of transistors onto a similar bite the dust. The more transistors there will be additionally exchanging and more power scattered as warmth or radiation. Warmth is one of the marvel bundling challenges in this age; it is one of the primary difficulties of low power plan procedures and practices. The expanding essentialness of convenient frameworks and the need to confine control utilization (and henceforth, warm dispersal) in high thickness Very Large Scale Integration (VLSI) chips have prompted fast and inventive improvements in low-control plan amid the current years. Flip-flops (FFs) are the fundamental stockpiling components utilized broadly in a wide range of computerized plans. Specifically, advanced plans these days frequently receive serious pipelining systems and utilize numerous FF-rich modules, for example, enroll record, move enlist, and first in first out. It is additionally assessed that the power utilization of the clock framework, which comprises of clock conveyance systems and capacity components, is as high as half of the aggregate framework control. FFs consequently contribute a huge segment of the chip territory and power utilization to the general framework plan. Another driver of low power look into is the dependability of the coordinated circuit. Additional exchanging infers higher normal current is ousted and thusly the likelihood of unwavering quality issues happening rises. We are moving from portable PCs to tablets and considerably littler figuring computerized frameworks. With this significant pattern proceeding and without a match slanting in battery future, the all the more low power issues should be tended to. The present patterns will in the end order low power plan computerization on an expansive scale to coordinate the patterns of energy utilization of the present and future incorporated chips. Power] utilization of Very Large Scale Integrated outline is given by

Summed up connection, P = CV2f [1]. Since control is corresponding to the square of the voltage according to the connection, voltage scaling is the most noticeable approach to diminish control scattering. In any case, voltage scaling is brings about limit voltage scaling which bows to the exponential increment in spillage control.

In spite of the fact that few commitments have been made to the specialty of single edge activated flip-flounders, a need clearly happens for a plan that further enhances the execution of single edge activated flip-flops designs. The design of a move enlist is very straightforward. A N-bit move enlist is made out of arrangement associated N information flip-flops. The speed of the flip-flop is less imperative than the territory and power utilization in light of the fact that there is no circuit between flip-flips in the move enroll. The littlest flip-tumble is reasonable for the move enlist to lessen the range and power utilization. As of late, beat locks have supplanted flip-

tumbles in numerous applications, on the grounds that a beat hook is considerably littler than a flip-flop. Be that as it may, the beat hook can't be utilized as a part of a move enlist because of the planning issue between beat locks.

2. RELATED WORK

A move enroll is the fundamental building obstruct in a VLSI circuit. Move registers are normally utilized as a part of numerous applications, for example, computerized channels, correspondence beneficiaries and picture preparing ICs Recently, as the extent of the picture information keeps on expanding because of the popularity for amazing picture information, the word length of the shifter enroll increments to process huge picture information in picture handling ICs. A picture extraction and vector era VLSI chip utilizes a 4K-bit move enlist A 10-bit 208 channel yield LCD segment driver IC utilizes a 2K-bit move enlist A 16-megapixel CMOS picture sensor utilizes a 45K-piece move enroll.

As the word length of the shifter enroll expands, the region and power utilization of the move enlist end up noticeably imperative outline contemplations. The littlest flip-slump is reasonable for the move enlist to lessen the territory and power Utilization. As of late, beat hooks have supplanted flip-flops in numerous applications, in light of the fact that a beat lock is considerably littler than a flip-tumble. Be that as it may, the beat lock can't be utilized as a part of a move enlist because of the planning issue between beat hooks.

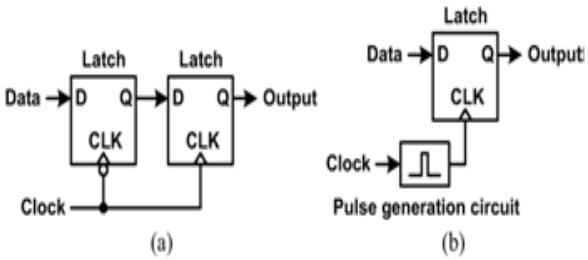


Figure 1: (a) Master-slave flip-flop. (b) Pulsed latch.

This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Shift registers can have both parallel and serial inputs and outputs.

These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also 'bidirectional' shift registers which allow shifting in both directions:

L→R or R→L. The serial input and last output of a shift register can also be connected to create a 'circular shift register' Previous work often measured energy consumption using a limited set of data patterns with the clock switching every cycle. But real designs have a wide variation in clock and data activity across different TE instances. For example, low power microprocessors make extensive use of clock gating resulting in many TEs whose energy consumption is dominated by input data transitions rather than clock transitions. Other TEs, in contrast, have negligible data input activity but are clocked every cycle. Shift registers, like counters, are a form of sequential logic. Sequential logic, unlike combinational logic is not only affected by the present inputs, but also, by the prior history. In other words, sequential logic remembers past events. Pulsed latch structures employ an edge-triggered pulse generator to provide a short transparency window. Compared to master–slave flip-flops, pulsed latches have the advantages of requiring only one latch stage per clock cycle and of allowing time-borrowing across cycle boundaries.

The major disadvantages of pulsed latch structures are the increased susceptibility to timing hazards and the energy dissipation of the local clock pulse generators

3. PROPOSED MODELLING

A master-slave flip-flop using two latches in Fig.1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b). All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.

The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift registers in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signals of the first latch (IN) is constant during the clock pulse width (TPULSE). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches.

However, the delay circuits cause large area and power over heads.

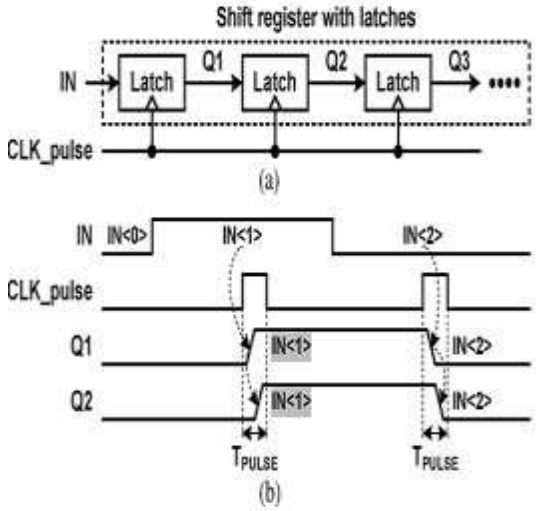


Fig. 2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b)Waveforms

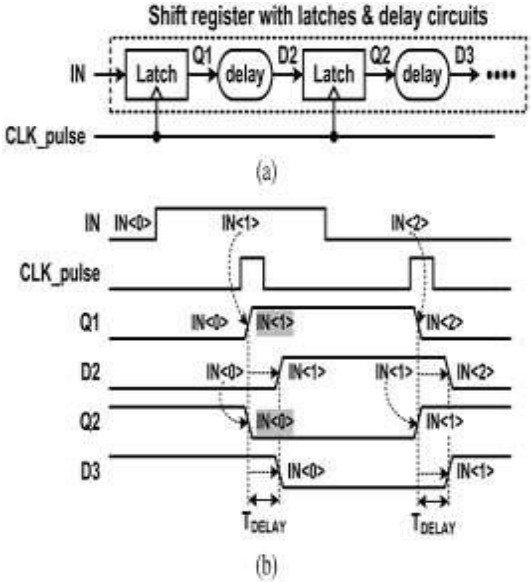


Fig. 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a)Schematic. (b)Waveforms

A 4-bitsub shifter register consists of five latches and it performs shift operations with five non overlap delayed pulsed clock signals (CLK_pulse<1:4>and CLK_pulse<T>). In the 4-bit sub shift register #1, four latches store 4- bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Fig. 4(b)shows the operation waveforms in the Proposed shift register.

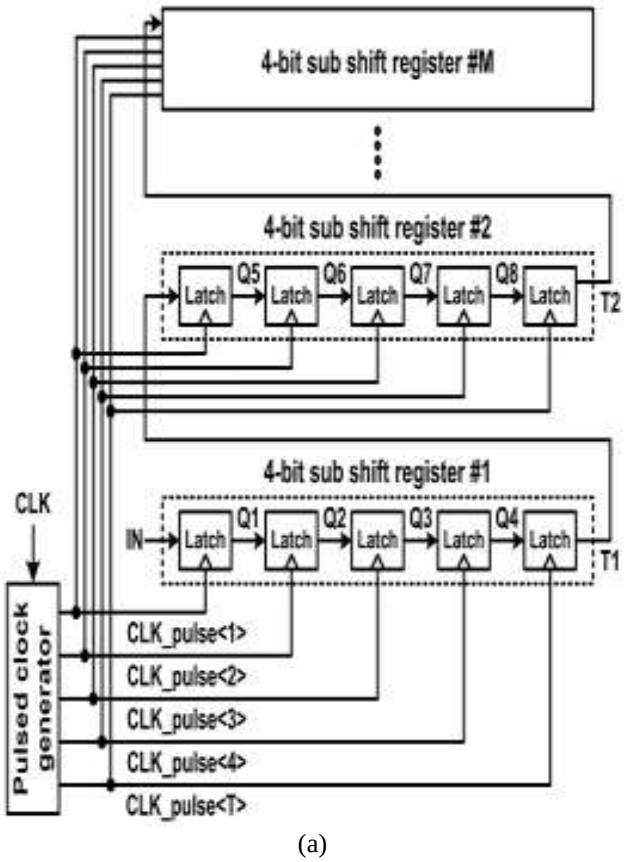


Fig . 4. Proposed shift register. (a) Schematic. (b) Waveforms.

The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register is selected by considering the area, power consumption, speed.

Area optimization: The area optimization can be performed as follows. Whenthe circuit areas are normalized with a latch, the areas of a latchand a clock-pulse circuit are 1 and , respectively. The total area becomes$(\alpha_A \times (K+1) + N\left(1+\frac{1}{K}\right)$. The optimal $K(=\sqrt{N/\alpha_A})$for the minimum area is obtained from the first-orderdifferential equation of the total area $(0=\alpha_A - N/K)$.An integer for the minimum area is selected as a divisor of, which is nearest to $\sqrt{N/\alpha_A}$.

Power optimization:

The power optimization is similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit

are1 and , respectively. The total power consumption is also $(\alpha_p \times (K+1) + N\left(1+\frac{1}{K}\right)$ .An integer for the minimum power is selected as a divisor of , which is nearest to $\sqrt{N/\alpha_p}$.

Chip Implementation:

The most extreme check recurrence in the regular move enrolls is constrained to just the deferral of flip-flops in light of the fact that there is no postponement between flip-flips. In this manner, the territory and power utilization are more vital than the speed for choosing the flip-flounder. The proposed move enroll utilizes hooks rather than flip-flops to decrease the region and power utilization.

4. SIMULATION RESULTS

SRAM is a type of semiconductor memory which is volatile in nature (retains the data as long as power is being supplied).It performs both read and write operations to store and fetch the data, based on the particular address. The read and write operations are controlled by the word line. Based on the bit line condition the data in it is stored and consists of a 1bit latch to store the data.

The 256bit pulsed latch shift register is used as part of SRAM in order to store the data in SRAM and fetch the data according to the given address location. So that it has low power consumption than the memory with general latch.

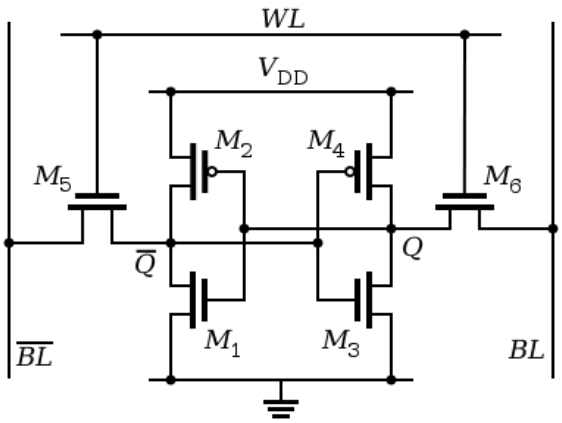
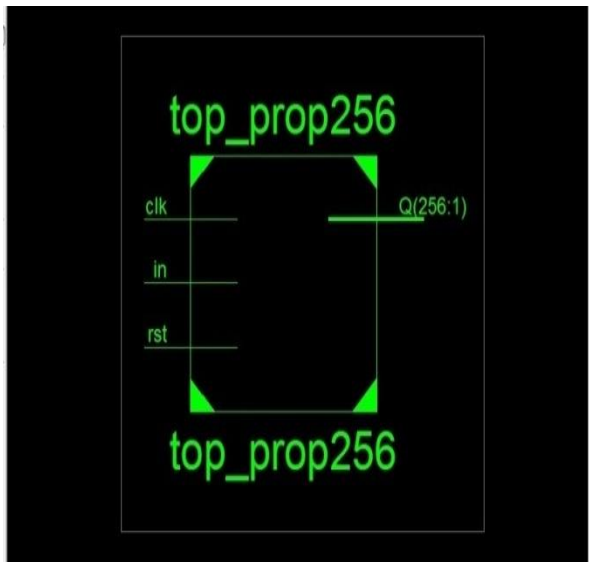


Fig. 5. 6T SRAM

Simulation Results

Top Module:

RTL Schematic:



Design Summary:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	186	4656	3%
Number of Slice Flip Flops	322	9312	3%
Number of 4 input LUTs	5	9312	0%
Number of bonded IOBs	259	66	392%
Number of GCLKs	6	24	25%

Timing Report:

```
Data Path: m65/m1/Q_1 to Q<253>
                              Gate     Net
  Cell:in->out      fanout    Delay    Delay  Logical Name (Net Name
  ----------------------------------------  ------------
   FDR:C->Q             1    0.514    0.357  m65/m1/Q_1 (m65/m1/Q_1
   OBUF:I->O                 3.169           Q_253_OBUF (Q<253>)
  ----------------------------------------
  Total                      4.040ns (3.683ns logic, 0.357ns route
                                     (91.2% logic, 8.8% route)
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5. CONCLUSION

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by substituting flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals as an alternative of a single pulsed clock signal.

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